

What is claimed is:

- 1 1. An apparatus comprising:
 - 2 a substrate;
 - 3 a target timing circuit formed on the substrate, the target timing circuit having
 - 4 a frequency related to a target frequency;
 - 5 a leakage timing circuit formed on the substrate, the leakage timing circuit
 - 6 having a frequency related to a leakage current; and
 - 7 a control unit to maintain a substantially constant ratio between the frequency
 - 8 related to the target frequency and the frequency related to the leakage current.
- 1 2. The apparatus of claim 1, wherein the substrate comprises a semiconductor.
- 1 3. The apparatus of claim 2, wherein the target timing circuit comprises a ring
- 2 oscillator coupled to a counter.
- 1 4. The apparatus of claim 3, wherein the leakage timing circuit comprises a ring
- 2 oscillator.
- 1 5. The apparatus of claim 4, wherein the frequency related to the leakage current
- 2 is substantially proportional to the leakage current.
- 1 6. The apparatus of claim 1, further comprising a self-timed circuit formed on
- 2 the substrate, the self-timed circuit to operate at a frequency proportional to the target
- 3 frequency.
- 1 7. The apparatus of claim 6, the control unit to provide a control signal to the
- 2 substrate.

1 8. The apparatus of claim 6, wherein the substrate includes a plurality of coupled
2 wells containing transistors of a matching type from the self-timed circuit, the target
3 timing circuit, and the leakage timing circuit.

1 9. The apparatus of claim 8, wherein the transistors are all of the matching type.

1 10. The apparatus of claim 9, further comprising a well control unit to provide a
2 bias to the plurality of coupled wells.

1 11. The apparatus of claim 10, wherein the well comprises a *p*-type well.

1 12. A system comprising:

2 a substrate;

3 a target timing circuit formed on the substrate, the target timing circuit having
4 a frequency related to a target frequency;

5 a leakage timing circuit formed on the substrate, the leakage timing circuit
6 having a frequency related to a leakage current;

7 a control unit coupled to a flash memory and to maintain a substantially
8 constant ratio between the frequency related to the target frequency and the frequency
9 related to the leakage current; and

10 a self-timed circuit formed on the substrate, and the self-timed circuit to
11 operate at a frequency proportional to the target frequency.

1 13. The system of claim 12, wherein the self-timed circuit comprises a memory
2 device communication interface.

1 14. The system of claim 12, wherein the self-timed circuit comprises a peripheral
2 device communication interface.

1 15. The system of claim 12, wherein the self-timed circuit comprises a network
2 communication interface.

- 1 16. An apparatus comprising:
- 2 a substrate;
- 3 a self-timed circuit formed on the substrate, the self-timed circuit to operate at
- 4 a target circuit frequency;
- 5 a target timing circuit formed on the substrate, the target timing circuit to
- 6 generate a signal having a frequency related to the target circuit frequency;
- 7 a leakage timing circuit formed on the substrate, the leakage timing circuit
- 8 having a leakage current and the leakage timing circuit to generate a signal having a
- 9 frequency related to the leakage current; and
- 10 a control unit to receive the signal having the frequency related to the target
- 11 circuit frequency and the signal having the frequency related to the leakage current
- 12 and to generate a control signal for application to the substrate, the control signal to
- 13 maintain a substantially constant ratio between the frequency related to the target
- 14 circuit frequency and the frequency related to the leakage current.
- 1 17. The apparatus of claim 16, wherein the substrate comprises silicon.
- 1 18. The apparatus of claim 17, wherein the target circuit comprises an interface
- 2 circuit.
- 1 19. The apparatus of claim 18, wherein the target ring oscillator comprises a ring
- 2 oscillator coupled to a counter.
- 1 20. The apparatus of claim 19, wherein the leakage ring oscillator comprises a
- 2 delay line.

- 1 21. An apparatus comprising:
 - 2 a substrate;
 - 3 a synchronous circuit formed on the substrate, the synchronous circuit to
 - 4 operate at a target circuit frequency;
 - 5 a target timing circuit formed on the substrate, the target timing circuit
 - 6 including voltage control, the target timing circuit to generate a signal having a
 - 7 frequency related to the target circuit frequency;
 - 8 a leakage timing circuit formed on the substrate, the leakage timing circuit
 - 9 including voltage control, the leakage timing circuit having a leakage current and the
 - 10 leakage timing circuit to generate a signal having a frequency related to the leakage
 - 11 current;
 - 12 a control unit to receive the signal having a frequency related to the target
 - 13 circuit frequency, the signal having a frequency related to the leakage current, and to
 - 14 generate a control signal for application to the substrate, the control signal to maintain
 - 15 a substantially constant ratio between the frequency related to the target circuit
 - 16 frequency and the frequency related to the leakage current;
 - 17 a power source to provide a potential to the synchronous, the target timing
 - 18 circuit, and the leakage timing circuit; and
 - 19 a potential control unit to receive the signal having the frequency related to
 - 20 the target circuit frequency and the signal having the frequency related to the leakage
 - 21 current and to generate a potential control signal to provide to the power source to
 - 22 adjust the potential.
- 1 22. The apparatus of claim 21, wherein the substrate comprises silicon.
- 1 23. The apparatus of claim 22, wherein the synchronous circuit comprises a
- 2 processor.
- 1 24. The system of claim 23, wherein the processor comprises a very long
- 2 instruction word processor.

1 25. The apparatus of claim 21, wherein the control unit includes a low-leakage
2 control signal to set the target circuit to a low leakage state.

1 26. A method comprising:
2 generating a first signal related to a target circuit frequency;
3 generating a second signal related to a leakage current; and
4 adjusting a control signal applied to a substrate to maintain a substantially
5 constant frequency ratio between the first signal and the second signal.

1 27. The method of claim 26, further comprising for a processor formed on the
2 substrate and having an operating frequency and a supply voltage, changing the
3 supply voltage to maintain a relationship between the target circuit frequency and the
4 operating frequency.

1 28. The method of claim 26, further comprising for a communications circuit
2 formed on the substrate, activating a transceiver in the communications circuit.

1 29. The method of claim 26, further comprising processing the target circuit
2 frequency and a target ring oscillator frequency to generate a potential control signal
3 to adjust a potential applied to a target ring oscillator, a leakage ring oscillator, and a
4 target circuit that operates at the target circuit frequency.

1 30. The method of claim 29, further comprising for a communications circuit
2 formed on the substrate, activating a transceiver in the communications circuit.